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I. SUMMARY AND CONCLUSIONS

Previous papers have presented simplified RF front-end and antenna preamp circuits for 100 KHz LORAN-C receivers (see "Mini-L LORAN-C Receiver" in 73 Magazine, April-May 1978). This report covers the circuit detail for a set of CMOS phase-locked loop boards and control system to convert the RF front end zero crossings to time difference navigation information. The system operates in the manual search-automatic tracking mode and is dependent on the quality of the RF input data. Two complete, portable, receiver systems have been fabricated. These are intended to provide mobile and airborne data collection apparatus for determining the precision of envelope-only sampling of the LORAN-C signals. The experimental hardware demonstrates that relatively simple receivers for marine use are possible with a precision of ± 1 microsecond. The receiver operator is required to monitor and position the LORAN-C signals with a small scope display system. Computer controlled automation of this manual search operation is the subject of continuing investigation.

The circuit details presented here may be of interest to other LORAN-C experimenters. The apparatus is not intended as a production prototype but rather as a demonstration of possible techniques which might be used in future receiver systems. The time difference readout technique used involves a single LSI counter chip with direct drive to an LED display. This method may be of interest for other types of LORAN-C processors with entirely different operational methods but with the same goal of determining a time interval between groups of pulses.

This report is intended to show at least one way of fabricating a simple LORAN-C receiver. Two models of this receiver have been fabricated and tested. Both have been used in portable automotive operation and in airborne tests with a microcomputer for altering the output TD information directly from the 8-pulse or GRI PLL outputs. Within the limitations of the RF front-end envelope deriver methods used, this hybrid analog VCXO-digital phase-locked loop technique can provide ± 1 μ sec precision when everything is properly adjusted. Future reports will present some of the navigation test results. The data presented here should provide sufficient detail to enable the skilled experimenter to utilize these techniques in other LORAN-C systems.

II. SYSTEM CONCEPT

Figure 1 is a block diagram of the system concept where it is assumed that an external RF front-end board provides a derived envelope suitable for observing on a scope display, and a 10 μ sec width pulse starting at some reproducible point on the envelope such as the ideal 30 μ sec sample point. Details of RF cycle delay and add envelope derivers using autocorrelation methods in the front end will be presented in other reports.

A 100 KHz phase locked-loop board is required for each LORAN-C station. A typical receiver would have three of these PLL boards, a common GRI-BCD switch, a

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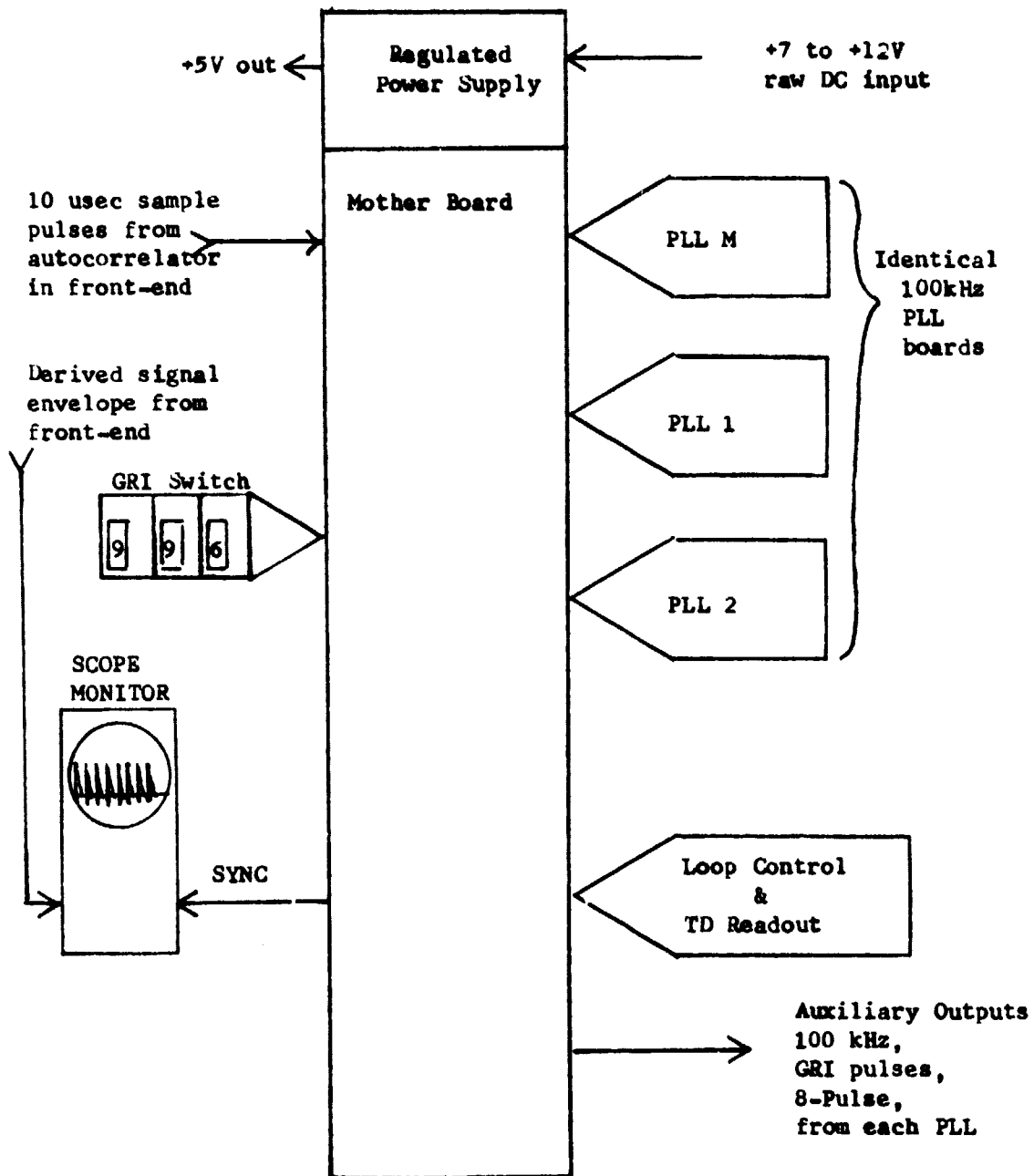


Figure 1. LORAN-C PLL Sensor Processor.

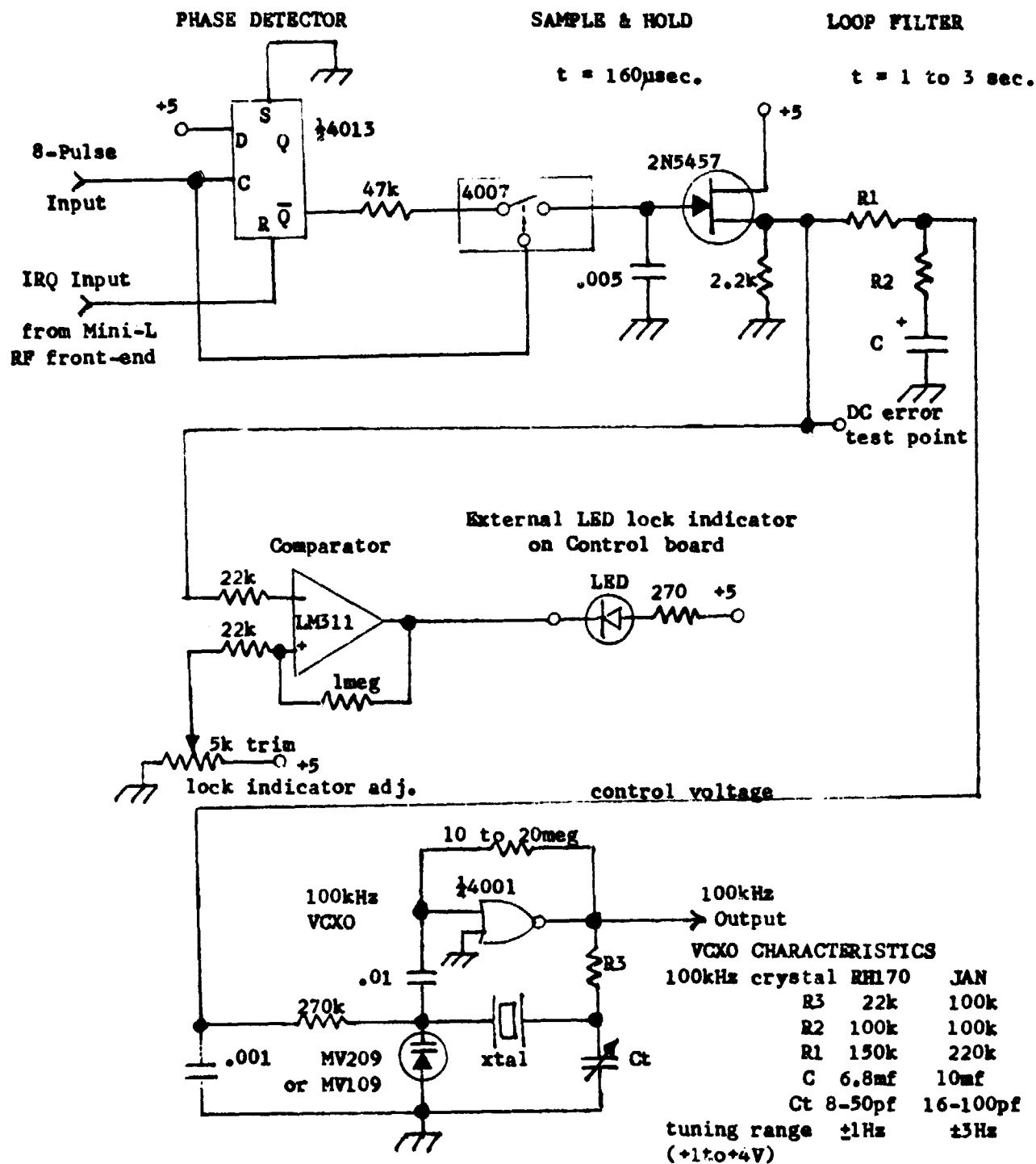
station selector for advance-retard positioning of each PLL, and a TD readout counter. A small triggered sweep scope such as the NLS MS-15 Miniscope is used as a signal acquisition aid. The receiver operates in the manual search-automatic tracking mode and can provide auxiliary outputs to drive external, computer-aided, navigation devices.

III. PHASE LOCKED LOOP BOARDS

Figure 2 is a diagram of a sample-and-hold phase detector and a 100 KHz VCXO (voltage controlled crystal oscillator). Each PLL board contains these circuits. The phase detector compares the position of the incoming LORAN-C samples with an 8-pulse replica (also generated later in the PLL board) and averages the resulting DC error voltage over 16-pulse groups or over two GRI periods. This DC signal is further filtered and used as the input error to the VCXO. The output of the VCXO on 100 KHz drives the count down chain and 8-pulse generator of Figure 3. The loop is locked when the LORAN-C pulses and the 8-pulse replica overlap just sufficiently to create enough DC error to keep the oscillator centered on 100 KHz. This is a first-order PLL system with a loop bandwidth of about 1 Hz. The 8-pulse replica ignores the phase code and the master 9th pulse. It consists of 10 μ sec pulses spaced exactly 1 ms apart, and repeating at whatever GRI rate is set on the BCD thumbwheel switches. The LSB decade ahead of the GRI decades is programmed to divide by 9, 10, or 11 to speed up or slow down each PLL. This allows positioning of each loop to agree with the incoming signal. The loop DC error signal operates a comparator to provide a lock indication when the signals are all lined up within the 8-pulse sample windows.

Obviously the most critical part of this circuit is the VCXO. 100 KHz watch size crystals obtained from Reeves-Hoffman provide a tuning range of about ± 1 Hz. Each VCXO is carefully offset to about 99999.5 Hz in the unlocked condition and the DC error increase pulls the oscillator higher in frequency to achieve lock. In assembling the PLL boards it is usually necessary to prepare a test jig with an accurate external variable DC source by opening up the loop from the phase detector output. Typical tuning characteristics as measured at the DC error test point ahead of the 270K isolating resistor (Figure 2) should be 99999.5 Hz for a low control voltage of 0.7 to 1.0V and a high reading of 100000.5 Hz for control voltages in the 2.5 to 3.0 volt range. It may be necessary to change the tuning capacitors to achieve this depending on the particular crystals used. Unfortunately the miniature watch-size crystals are not generally available except in quantity orders of 100 or more. JAN, USCC, and Bliley 100 KHz, standard size, crystal units have also been used in one of the receivers with reasonable success.

A possible circuit board layout and parts overlay diagram are illustrated in Figures 4 and 5 for the PLL boards. The 4029 counter chips may be changed to 4510 types except for the LSD which requires a binary mode 4029 or 4516. If the 4516 is used it is necessary to break one foil jumper to pin #9 and ground this pin to #10. The board layout is prepared assuming the use of 4029 chips for all counter stages. A 100 KHz output is available from each PLL board for external use as a source for checking frequency counters and timers when the loop is locked to LORAN-C. A GRI test point is also on each board.



MINI-L PLL CIRCUIT

Figure 2. Phase Detector and VCXO.

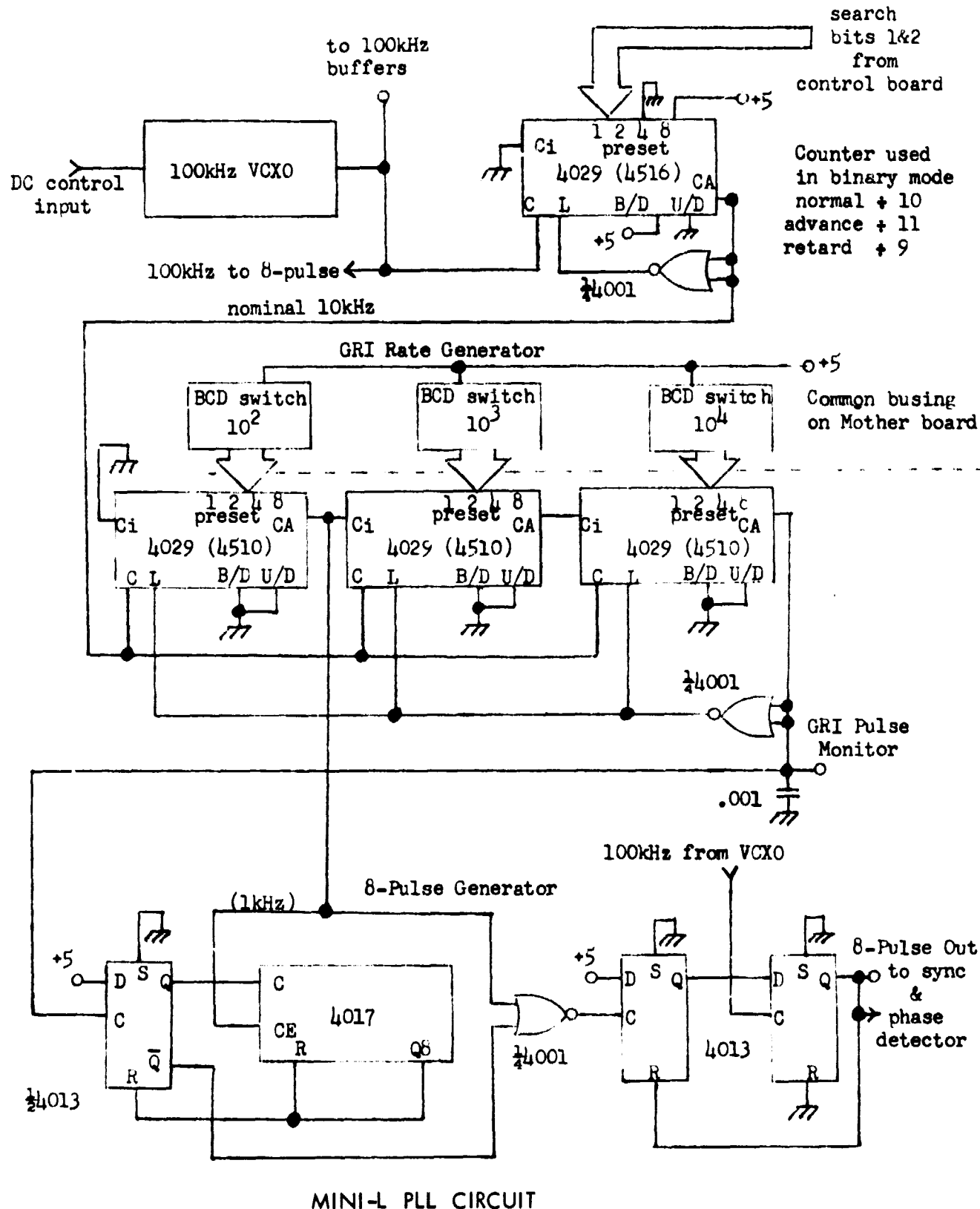


Figure 3. GRI and 8-Pulse Generator.

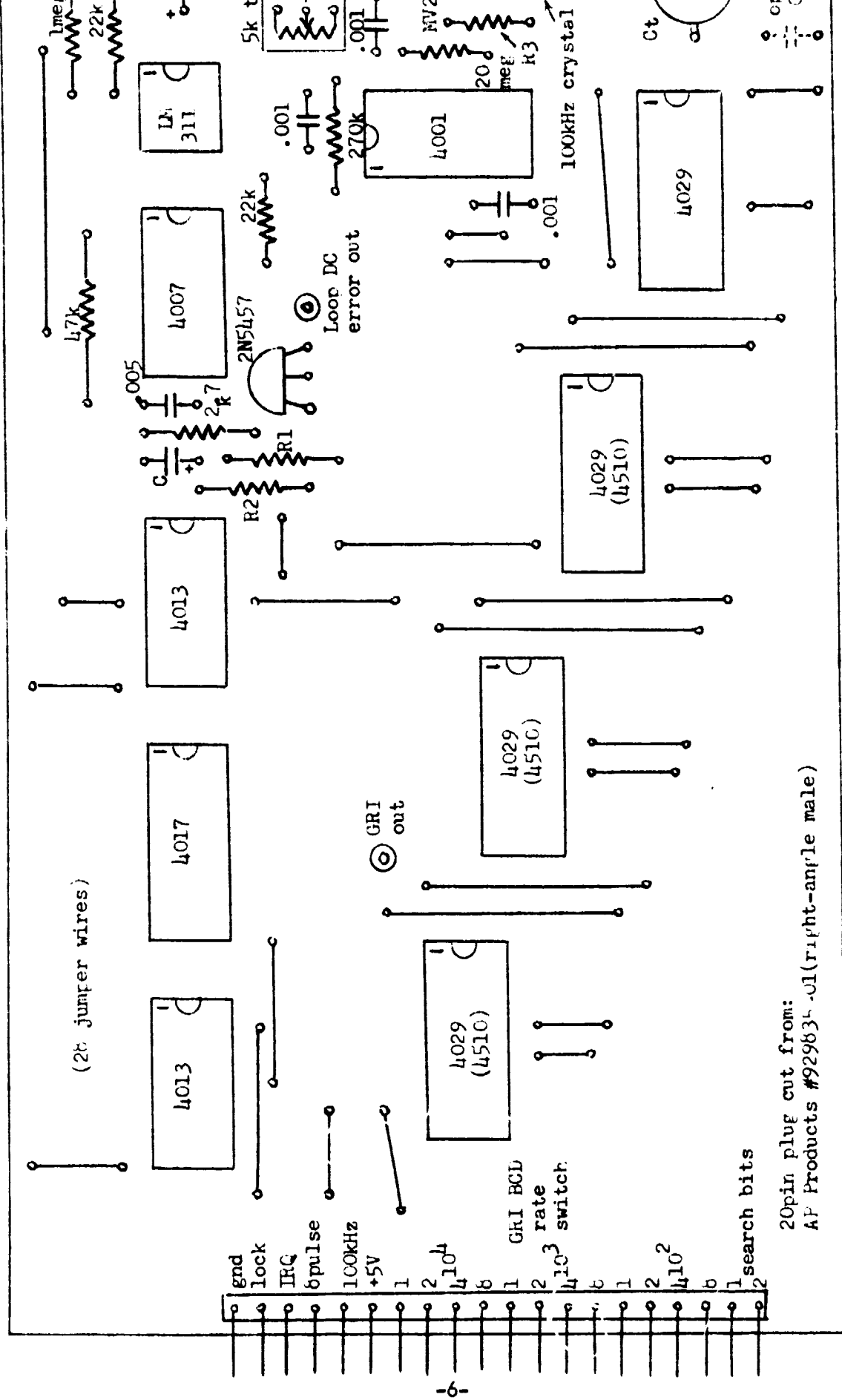
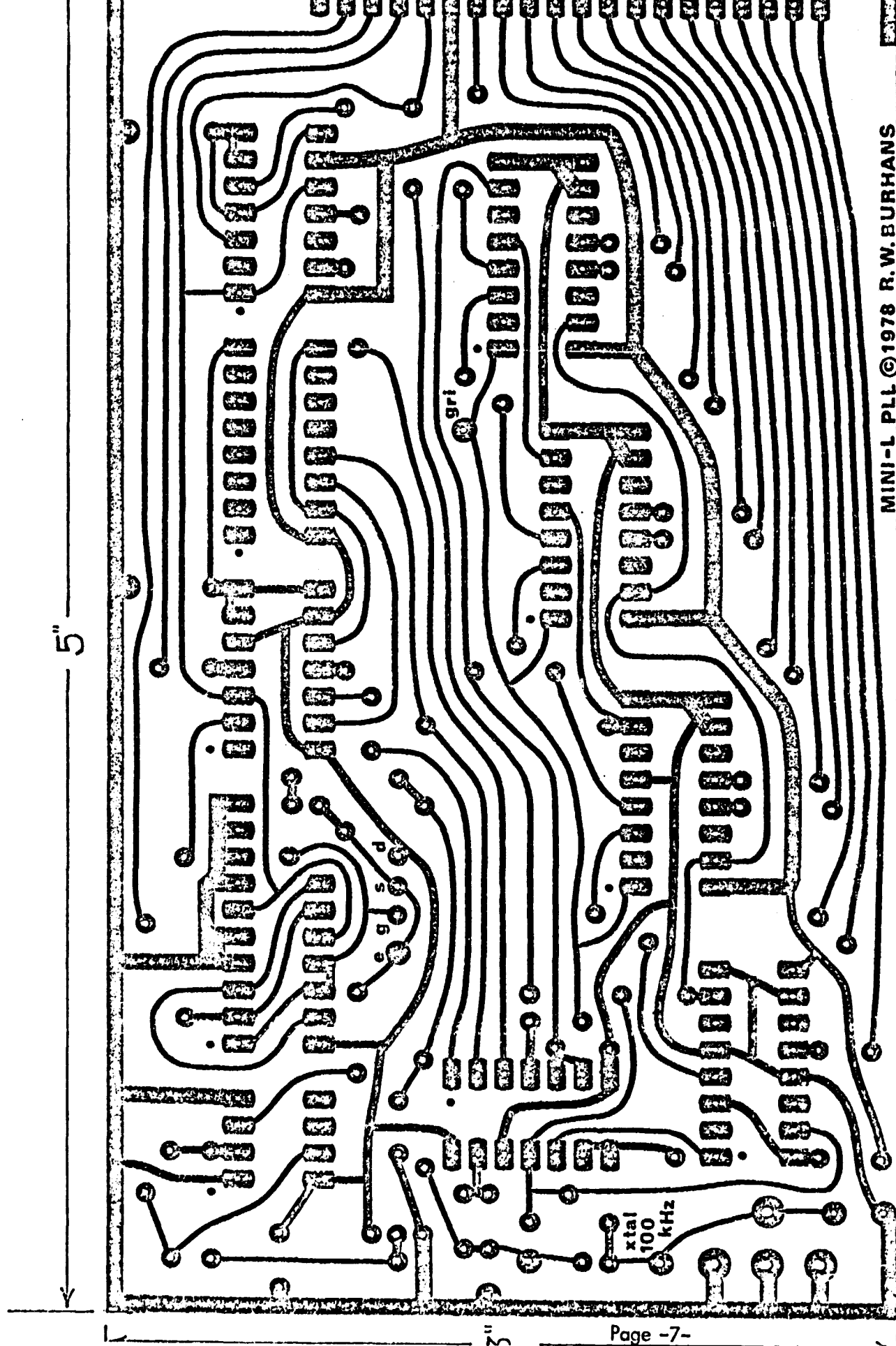


Figure 4. Mini-L Phase Locked Tracking Loop, Component Side.



MINI-L PLL ©1978 R.W.BURHANS

Figure 5. PLL PC Layout.

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The GRI pulse occurs before the 8-pulse output by exactly whatever is programmed on the GRI switch LSD section. Thus for a GRI rate of 99300 μ sec the GRI pulse anticipates the 8-pulse group by 300 μ sec. This might be of value in external computer-aided data reduction of the TD data and in automatic search after loss of lock for future computer-aided systems.

The phase code averaging method used here may cause some problems when low-level or noisy signals are sampled. This problem is the subject of further investigation with the ultimate goal of substituting an all-digital or DPLL system with a common 1 MHz oscillator and adding or subtracting pulses from the first counting stage to achieve lock. The hybrid method using 100 KHz VCXOs has the advantage of minimizing the chip count per loop in the present implementation.

IV. MOTHER BOARD

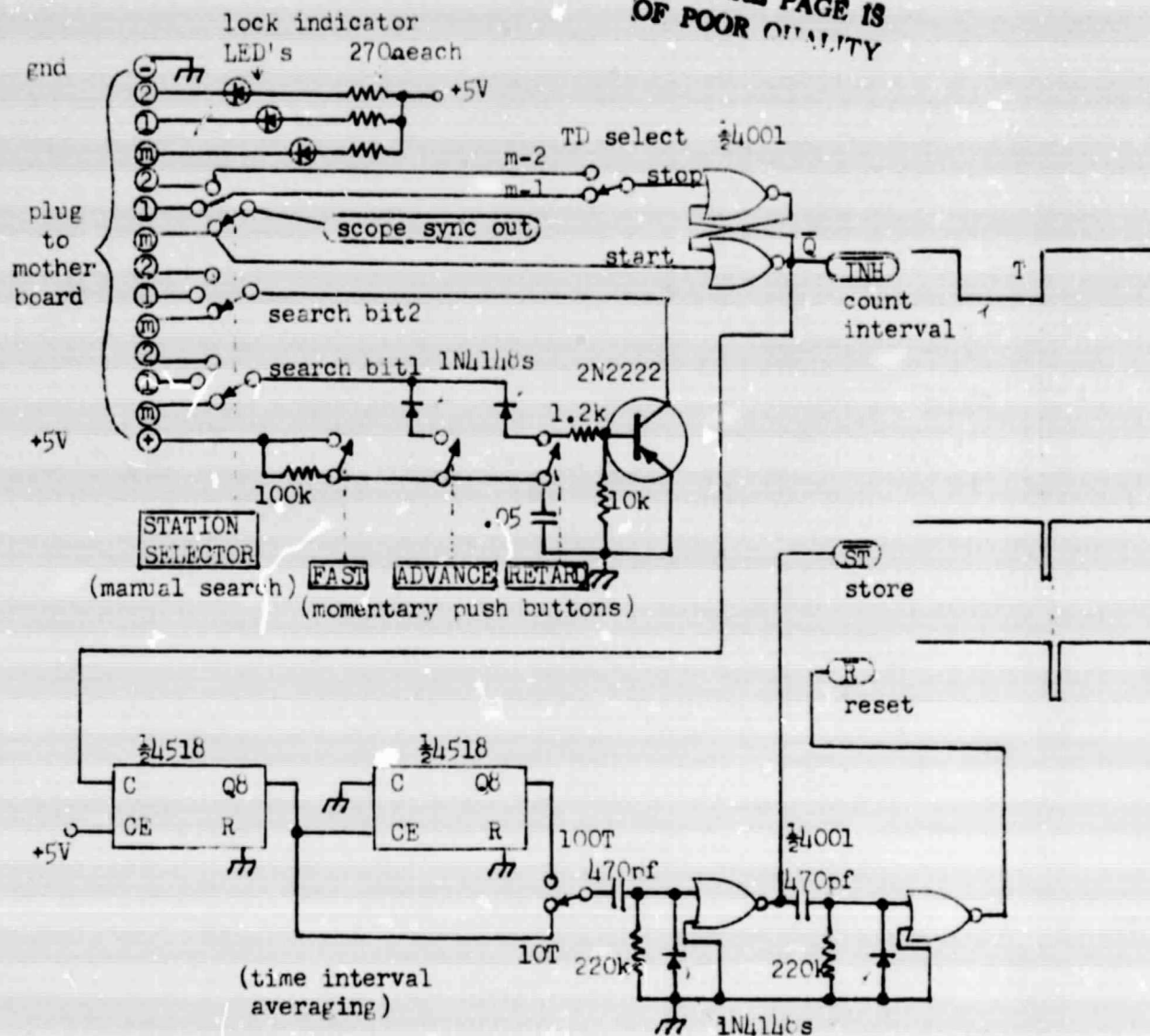
Three of the PLL boards are intended to plug into a mother board which contains a power supply regulator, socket strips, provision for a common BCD GRI switch, and a socket to plug in the control and TD readout circuit board. A buffer amplifier is also provided on the board (Figure 6 overlay diagram) which is shown wired for 100 KHz outputs, but other signals such as the GRI or 8-pulse could be brought out with a few minor changes on each of the PLL boards. The BCD decade switch is terminated with 22K resistors to ground so that a simple +5V common wire to each switch section provides the proper BCD code at each PLL terminal strip in parallel. Two of the binary divider bits are also brought out and commutated on the mother board so as to provide a set of wires to control each PLL independently on the control board. An LED indicator lead from each PLL is similarly routed to the control board, and the 8-pulse lead is wired through the selector switch to enable checking each PLL independently with a monitor scope. A PC board layout of the mother board is illustrated in Figure 7.

V. CONTROL AND TD DISPLAY BOARD

One of the slots (labeled m) on the mother board is reserved for the master station PLL, and a toggle switch on the control board wired to use either of the other two PLL slots as an off or stop signal for the TD counter. Figure 8 is a diagram of the control circuit. The first master 8-pulse event starts the time interval flip-flop and the 1st slave selected stops the flip-flop, providing a time interval. The interval is filled with 1 MHz pulses from a crystal oscillator through gating inside the Intersil 7208 counter chip shown in Figure 9. Either 10 or 100 of these intervals of 1 MHz pulses can be hardwired on the control board to provide the total time interval count to the 7208 IC. The count is stored in the counter chip after each 10 or 100 time intervals and the counter reset for the next series of intervals. Thus, at GRIs in the 9930 range the counter will update about once per second in the divide by 10 or 10T mode. Similarly the counter will update about every 10 seconds in the 100T mode. Pads are provided on the control board so that the user can wire an additional T-selector toggle switch and change the decimal point as well as the count mode. One receiver was hardwired with a permanent 10T, and in the other a DPDT switch was used.



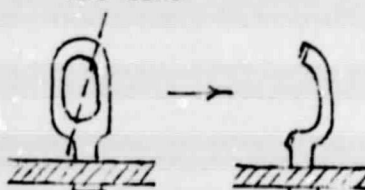
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Original Switch

cut line

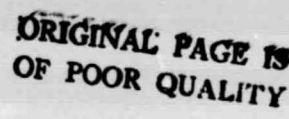
Modified Contacts



Mouser 10 WW 033
3-pole, 3-position
switch for PC mount

MODIFIED SELECTOR SWITCH FOR PC BOARD

Figure 8. Mini-L Control Circuit.



-12-

The 1 MHz crystal oscillator provides the reference which should be set to much better than 10 Hz to provide 1 microsecond timing precision within each GRI interval. The counter will actually read to 0.1 μ sec because of the period averaging in the 10T mode (or to 0.01 microseconds in the 100T mode). However, it is wise not to trust these fractional readings unless very tight PLL circuits are used and high precision insured in the RF front-end sampling. The 100T mode helps in averaging out the cross rate interference problem. Extra pads are provided for capacitors near the 1 MHz oscillator so that a variety of 1 MHz crystals might be trimmed to the correct frequency or even temperature compensated in series or parallel with suitable TC or NPO capacitors. At some future time it is planned to make this same crystal oscillator the reference for an all-digital DPLL system by changing the PLL boards and using the same mother board and control-TD readout system with only minor changes. A parts layout is illustrated in Figure 10 with the PC foil layout shown in Figure 11.

VI. MECHANICAL DETAILS

The control board is intended to be mounted parallel to a panel with the 3-section (Mouser 10WW033) 3-pole selector switch nut as the primary support. Additional support can be provided by suitable locating the toggle and push button switches. Other arrangements are possible, including mounting the control board well away from the panel, and using a wiring harness to panel mounted control elements. The front panel should contain some form of gain control for the front-end, a power on-off switch, and coaxial fittings for the envelope monitor output and sync. terminal from Figure 8.

One problem experienced is that of failure of the momentary pushbutton switches after a few thousand operations. We finally ended up with some more expensive Grayhill switches and used good quality miniature toggles selling in the \$1.50 range. The extra cost is well worth the improved performance. In assembling the board and panel, care should be taken to avoid overtightening nuts on switches so as to prevent panel warping in case of misalignment of the holes.

In wiring up a complete system, some form of metal box is preferred to provide some shielding. The envelope output from the front-end and the 8-pulse output can be fed back into the front-end, creating all sorts of problems in open breadboard layouts with no electrostatic isolation of the antenna and preamp. Electromagnetic radiation is also a problem sometimes as in the case of a nearby TV set horizontal oscillator which radiates a strong 6th harmonic component right in the middle of the LORAN-C band. In both of the receivers fabricated, the front-end board was mounted to the rear of the box, well grounded to the chassis, with the PLL assemblies and control board to the front. There is no cross-talk problem with the low power CMOS at the low impedance RF board input. However, the preamplifier must be isolated with a length of coaxial cable back to the main receiver such that it is well outside the "Faraday Cage" formed by the vehicle and the receiver processing box.

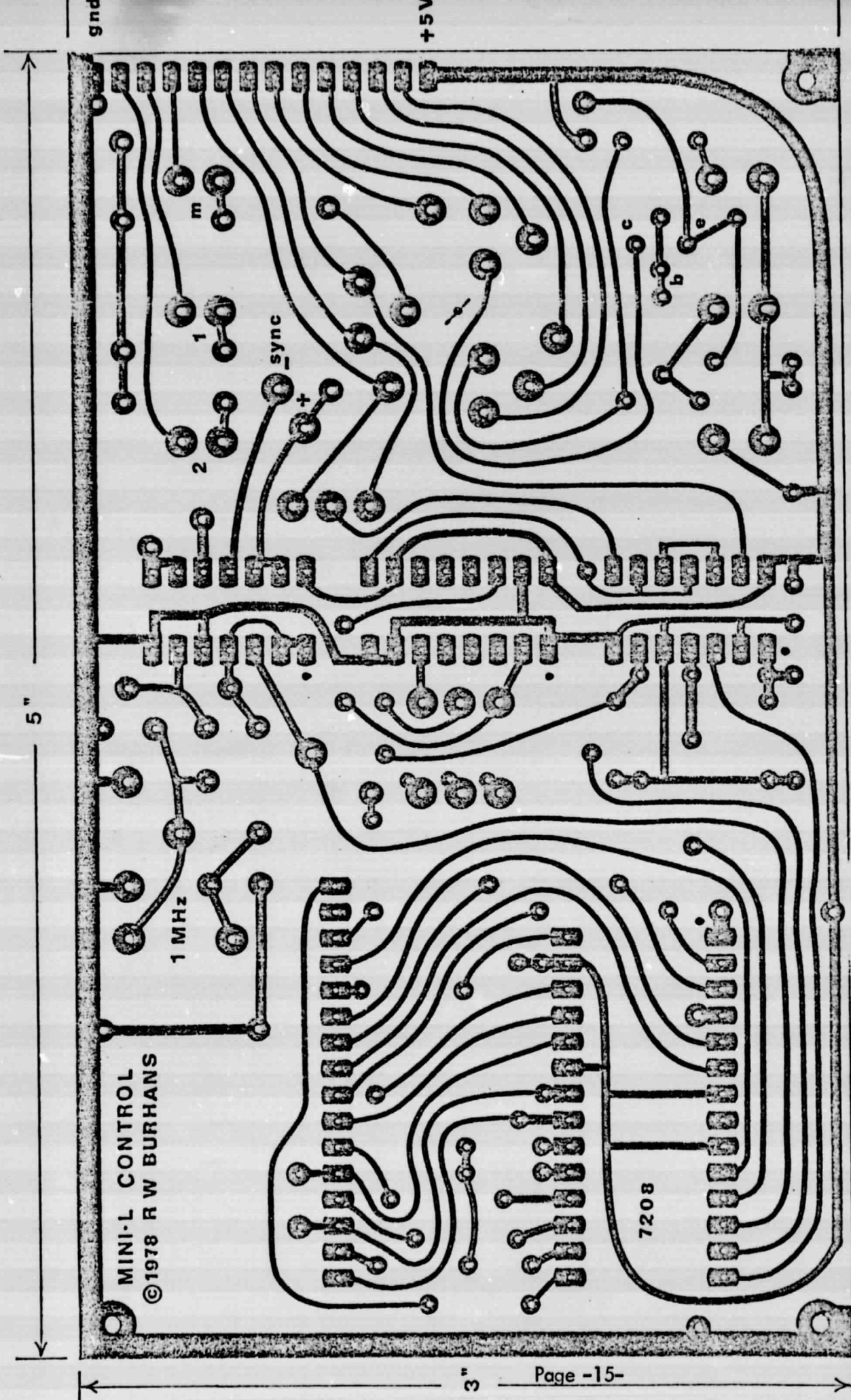


Figure 11. Control and TD PC Layout.

VII. RECEIVER OPERATION

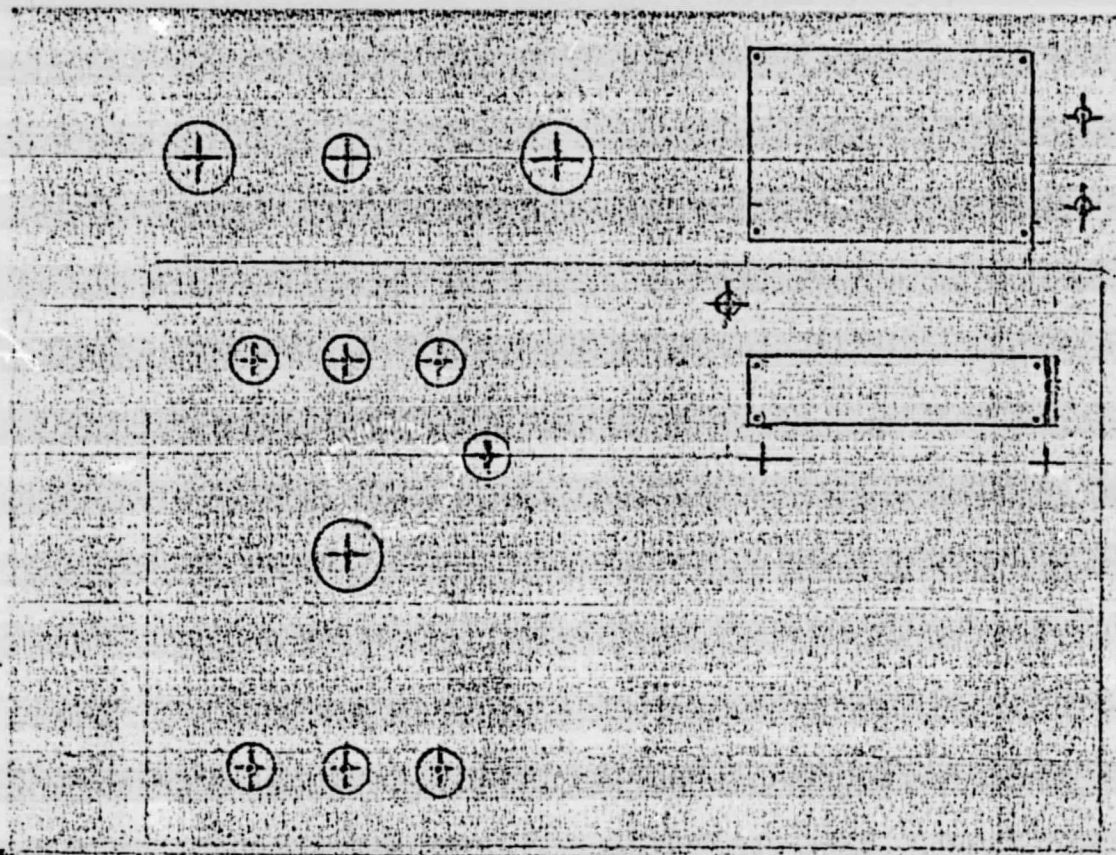
Operation is quite simple. The station selector is turned to the master position and the advance-retard buttons operated until the master station is locked on the left edge of the scope by observing the lock indicator LED. Each desired slave station is similarly positioned. The TD counter then starts reading time differences between selected station pairs directly in microseconds. A fast-normal switch allows rapid slewing of the stations in the search mode and a normal slew rate of only 50 μsec per button push when near the correct point. The PLL circuits are offset about 0.5 Hz such that they will slew to lock at about 5 $\mu\text{sec}/\text{sec}$ when approaching lock. We usually bring the stations to within 50 μsec of the left edge of the scope trace and then let the loops automatically come to lock (about 10 seconds to 50 seconds depending on the sample point selected from the front-end).

VIII. ACKNOWLEDGEMENTS

This work has been supported by NASA Langley Research Center, Grant NGR 36-009-017. The aid of student assistant Ed Jones is particularly appreciated during the experimental fabrication and debugging parts of the project effort. Others assisting in the data collection and analysis phase have been Dr. Robert W. Lilley, and students Jim Nickum, Joe Fischer, and Lynn Piecuch.

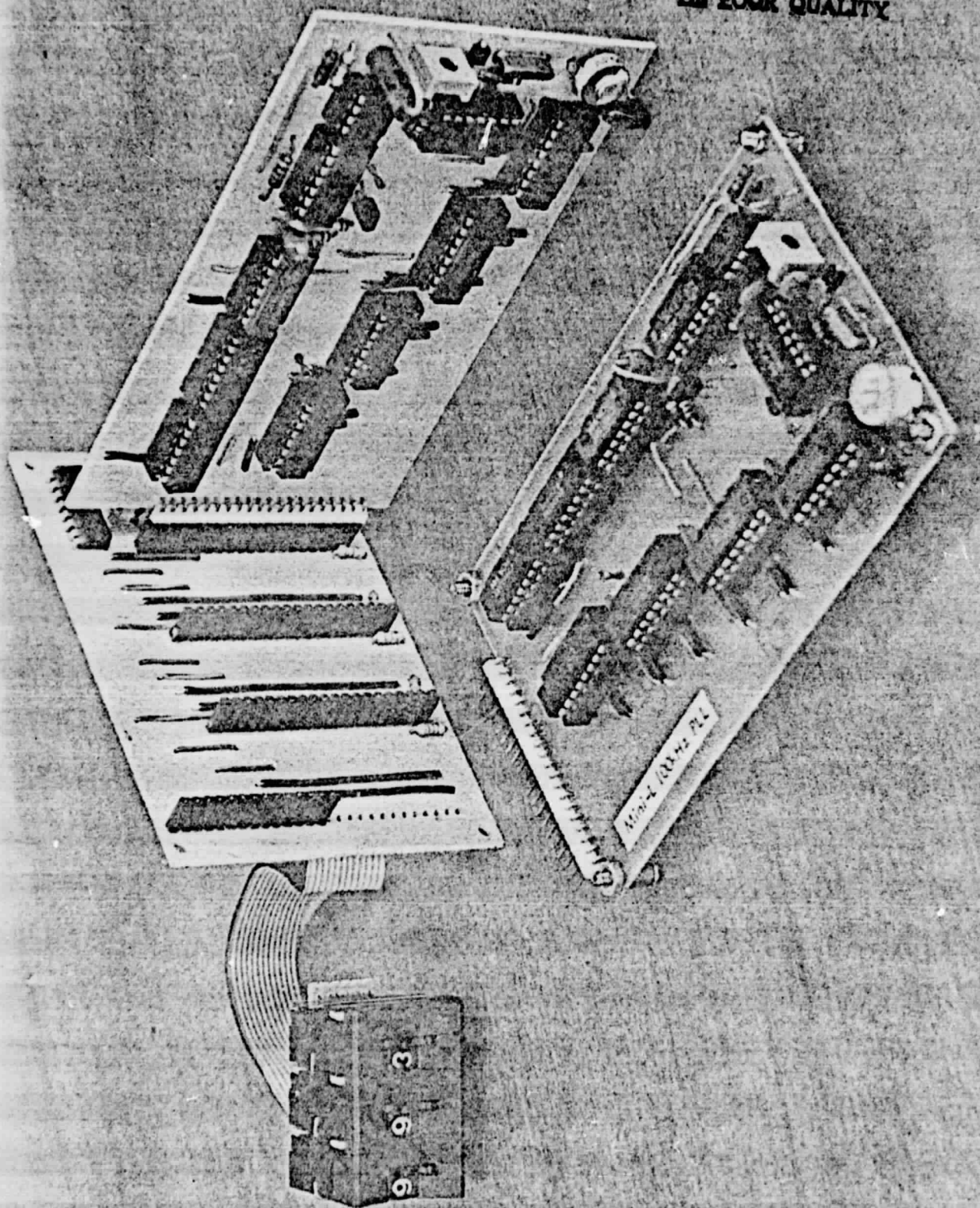
IX. APPENDICES

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MINI-L PANEL LAYOUT SKETCH (Full size layout)
For LMB type CR-864 box assembly

Figure A-1. Front Panel Sketch.



PLL BOARDS, MOTHER BOARD, GRI SWITCH (Control Board not shown)

Figure A-2. Photograph of PLL and Mother Board.

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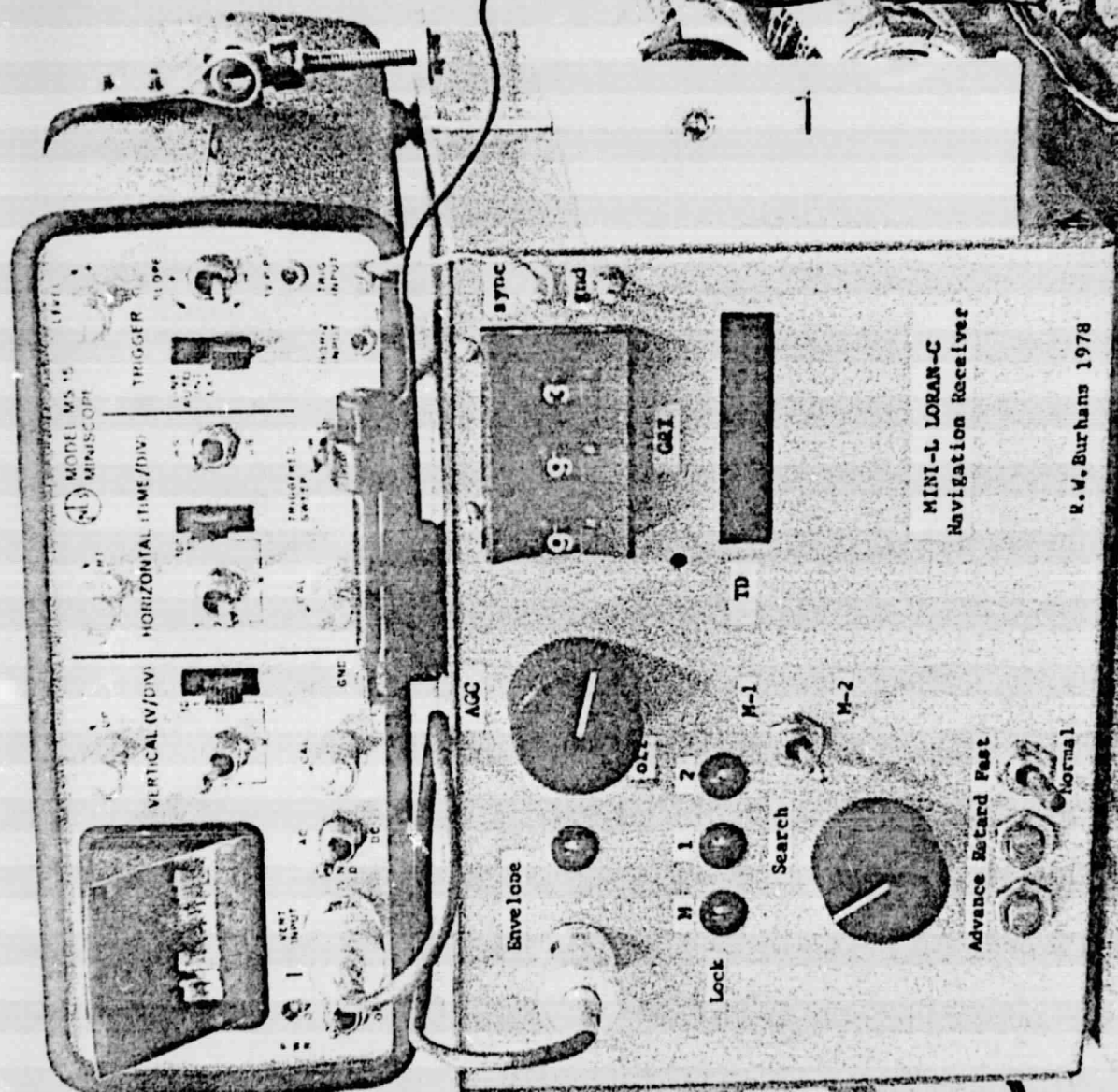
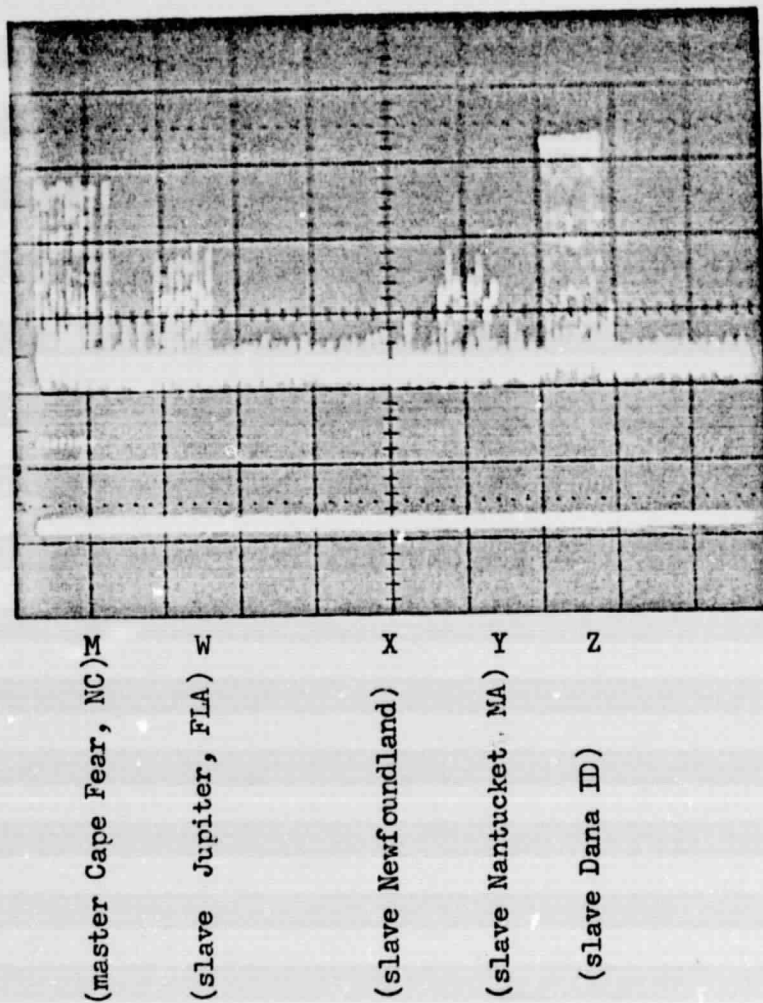


Figure A-3. Photograph of Complete Receiver.

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MINI-L
ENVELOPE OUT

8-PULSE
OUTPUT



MINI-L PLL LOCKED TO MASTER STATION
EAST COAST LORAN-C CHAIN, 99300 GRI

Figure A-4. Photograph of PLL Locked to Master.